Abstract of the Disclosure

[0041] Dynamic phase alignment circuitry selects from among several, phase-distributed, candidate clock signals the one of those signals that is currently best for use in controlling the timing of sampling of a serial data signal to recover the data from that signal. The circuitry selects two phase-adjacent ones of the candidate clock signals that are currently the two best candidates for final selection. The circuitry makes a final selection of the generally better one of these two best candidates in a way that avoids unproductive switching back and forth between these two best candidates.